

Form PTO-1449 (modified)

Atty. Docket No.

2000.052000/TT4034

Serial No.

10/066,948

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Applicant

DALE E. GULICK

Filing Date:

Feb. 4, 2002

Group:

2184

U.S. Patent Documents

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Foreign Patent Documents

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Other Art

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U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						
	A3						
	A4						
	A5						

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Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						
	B3						
	B4						
	B5						

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)
	C2	Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99)
	C3	Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)
	C4	FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)
	C5	"Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, 203 - 212

EXAMINER:

Thomas M. J. Smith

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8/16/03

EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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See Page 1Foreign Patent Documents
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	C7	Intel, "Advanced Configuration and Power Interface Specification," Revision 1.0b, 02/02/1999
	C8	Intel, "Advanced Configuration and Power Interface Specification," Revision 2.0, 07/27/2000
	C9	Intel, "Advanced Configuration and Power Interface Specification," Revision 2.0 Errata, Errata Document Rev. 1.5, 04/13/2001
	C10	Case, Pedor, Schoffstall, Davin, "A Simple Network Management Protocol (SNMP)" May, 1990
	C11	"Network Device Class Power Management Reference Specification," Version 2.0, 10/12/2000 pp. 1-9
	C12	Intel, "IPMI Intelligent Platform Management Interface Specification v 1.0," Document Revision 1.0, 09/16/1998
	C13	Intel, "IPMI Intelligent Platform Management Interface Specification v 1.5," Document Revision 1.0, 02/21/2001
	C14	Intel, "IPMI v 1.5 Addenda, Errata, and Clarifications - Intelligent Platform Management Interface Specification v1.5, revision 1.0," Addendum Document Revision 3, 05/16/2001
	C15	Intel, "IPMI Platform Management FRU Information Storage Definition v1.0," Document Revision 1.0, 09/16/1998
	C16	Socolofsky et al., "A TCP/IP Tutorial," January 1991
	C17	Intel, "IPMI Platform Management FRU Information Storage Definition v1.0, Document Revision 1.1, 09/27/1999
	C18	Intel, "Meticulous ACPI/Manageability," Specification v1.0, 04/30/1999
	C19	Intel, "IPMI Intelligent Platform Event Trap Format Specification v 1.0," Document Revision 1.0, 12/07/1998
	C20	DMTF, "Common Information Model (CIM) Specification," DSP0004, Version 2.2, 06/14/1999
	C21	Intel, "SMBus Control Method Interface Specification," Version 1.0, 12/10/1999

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	C22	Intel, "System Management BIOS Reference Specification," Version 2.3.1, March 1999
	C23	Intel, "System Management Bus Specification," Revision 1.0, 02/15/1995
	C24	Intel, "System Management Bus (SMBus) Specification," SBS Implementers Forum, Revision 2.0, 08/03/2000
	C25	J. Postel, "User Datagram Protocol," ISI 08/28/1980
	C26	"About the 8051 Microcontroller," pp. 1-16
	C27	Intel, "8259A Programmable Interrupt Controller (8259A/8259A-2)," December, 1988
	C28	Intel, "Intel® 840 Chipset Platform Design Guide," October, 1999
	C29	AMD, "AMD's Altera™ Technology for Advanced Systems Management," Publication No. 22297 Rev. A, December, 1998
	C30	AMD, "AMD-766™ Peripheral Bus Controller Data Sheet," 23167B March, 2001

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